REMARKS

Claims 1-33 remain pending in the application. Claims 1, 8, 12, 22, 24, 25, 26, 29, and 31 have been amended.

Objections to the Drawings:

The drawings were objected to. In a first objection, the Examiner states that the LSSD clocks and STEP clocks shown in Figure 2 are not referred to in the disclosure. Applicant respectfully disagrees, and submits that both the LSSD clocks (also shown as LSSD_CLKA and LSSD_CLKB in Figure 9) and the STEP clocks (shown in Figure 9 as the clock signals of LBST_STEP_CLKC and LBST_STEP_CLKE) are referred to in the paragraph beginning on page 10, line 6, in conjunction with Figure 9.

The drawings were also objected to because the LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SCAN_CLKB were not referred to in the disclosure. Applicant has amended the disclosure to include reference to the LSSD_CLKA and LSSD_CLKB signals, which are the LSSD clocks discussed above. Applicant has amended Figure 9 to remove the LBST_SCAN_CLKA and LBST_SCAN_CLKB references.

Objection to the Specification:

The specification was objected to for various informalities. Applicant has amended the specification to correct these informalities.

35 U.S.C. § 112 Rejection:

Claims 23, 26, and 30 were rejected under 35 U.S.C. § 112, second paragraph. With respect to claims 23 and 30, Applicant has amended the claims upon which these claims depend, thereby establishing antecedent basis. With respect to claim 26, Applicant submits that the amended version of this claim is in compliance with 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 103 Rejections:

Claims 1, 3, 5, 8, 10, 22, 24 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara, U.S. Patent 6,629,281, in view of Kim, U.S. Patent 5,938,784. Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Simpson, U.S. Patent 5,260,950, Wong, U.S. Patent 6,636,997, and Bogholtz, U.S. Patent 5,357,523. Claims 7, 11, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, and in further view of Rajski, U.S. Patent 5,991,909. Claims 6, 12, 14, 16, 17, 18, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Motika, U.S. Patent 5,982,189. Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Motika and Bardell, U.S. Patent 4,959,832. Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Motika, Simpson, Wong, and Bogholtz. Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim, U.S. Patent 6,148,426 ('Kim 2'). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Motika and Au, U.S. Patent 6,681,359. Claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, and in further view of Motika and Rajski. Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and in further view of Wong and Bogholtz. Claims 29, 31, 32, and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski and in further view of Kim. Claim 30 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski, Kim, and Bardell. Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. McNamara describes a method and apparatus, contained within an integrated circuit, for isolating failure by precisely controlling the number of clocks applied during built-in self-test (BIST). A programmable clock counter, on the integrated circuit, stores a specified number of clock cycles and sends a signal to stop a BIST engine once the specified number of clock cycles

have been generated. The intermediate results can then be mapped bit by bit in order to isolate the cause of failure.

Kim teaches a built-in self test (BIST) circuit using a linear feedback shift register (LFSR) and a multiple input signature register (MISR) requiring reduced circuitry exclusive of the number of inputs and outputs of the circuit to be tested. The BIST circuit is built in a prescribed circuit having a memory to test a target circuit in the prescribed circuit. The BIST circuit includes an LFSR, including a first logic section which is composed of a plurality of XOR gates and selection sections, and a first memory which is a part of the memory, for performing a primitive polynomial, an MISR, including a second logic section which is composed of a plurality of XOR gates and selection sections, and a second memory which is a part of the memory, for performing the primitive polynomial, and a BIST control section for controlling data input/output between the first and second memories and the target circuit and providing selection signals for controlling the selection sections in the first and second logic sections, the BIST control section controlling the target circuit and comparing operation results of the target circuit to perform the test of the target circuit.

In contrast, Applicant's independent claim 1 recites, in pertinent part:

> "A built-in self-test controller, comprising ... a pattern generator seeded with a first primitive polynomial; and a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number." (Emphasis added).

Independent claims 8, 12, 22 and 29 recite similar combinations of features.

Neither McNamara nor Kim, taken singly or in combination, teach or suggest this combination of features. In particular, Applicant can find no teaching or suggestion in either of the cited references of a pattern generator seeded with a first primitive polynomial and storing the contents of a logic built-in self-test per a second primitive polynomial, wherein the first primitive polynomial and the second primitive polynomial have a different number of bits. In the Office Action, the Examiner states that that Kim teaches an LFSR (pattern generator) and a MISR, both being based on primitive polynomials (Abstract, column 1 lines 33-59, column 2 lines 1-6 and lines 20-67, and column 4, lines 1-28). Applicant can find no teaching anywhere in these citations, elsewhere in Kim, or in any of the cited references, of a first polynomial having a first number of bits and a second polynomial having a second number of bits, wherein the second number is different from the first number, as recited in the independent claims.

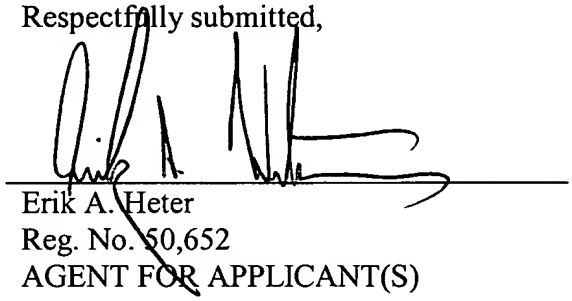
Accordingly, Applicant submits that the combination of McNamara and Kim does not render the independent claims obvious. With respect to the remaining rejections and the cited references, Applicant submits that the independent claims are not rendered obvious for at least the same reasons. Accordingly, removal of the 35 U.S.C. § 103(a) rejections is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-55500/BNK.

Respectfully submitted,



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Date: June 8, 2004